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(54) Title of the Invention

MEMORY DEVICE AND ITS RECORDING/ REPRODUCING METHOD

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Specification

I. Title of the Invention

Memory Device and Its Recording/Reproducing Method

II. Claims

Claim 1.

A memory device, characterized by having a piezoelectric body layer exhibiting piezoelectric characteristics,
a ferroelectric body layer laminated on one side of the piezoelectric body layer and laminated so as to transmit stress generated by the inverse piezoelectric effect of the piezoelectric body layer,
writing electrodes arranged opposing one another by interposing the ferroelectric body layer and generating an electric field for polarizing the ferroelectric body layer into a polarized state corresponding to information to be stored, and
reading the electrodes arranged to oppose one another by interposing the piezoelectric body layer and generating an electric field of a magnitude which generates stress to the extent that it does not destroy the polarized state of the ferroelectric body layer.

Claim 2.

The memory device according to Claim 1, characterized by making the electrode pieces of the writing electrodes and the reading electrodes arranged between the piezoelectric body layer and the ferroelectric body layer to be common electrode pieces.

Claim 3.

The memory device according to Claim 1, characterized by the fact that the writing electrodes and the reading electrodes comprise stripe-shaped electrodes that are perpendicular to each other between both respective sides of the piezoelectric body layer and the ferroelectric layer,
where the portion where the stripe-shaped electrode pieces formed on one side of the ferroelectric body layer and the stripe-shaped electrode pieces formed on the other side of the ferroelectric body layer intersect each other is adopted taken as the memory cells,
and where the portion where the stripe-shaped electrode pieces formed on the one side of the piezoelectric body layer and the stripe-shaped electrode pieces formed on the other side of the piezoelectric body layer intersect each other are adopted as piezoelectric cells, the laminated paired memory cells and piezoelectric cells being arranged into a matrix.

Claim 4.

The memory device according to Claim 3, characterized by laminating multiple layers of the memory cells.

Claim 5.

The recording/reproducing method of the memory device according to Claim 1, characterized by the fact that positive or negative pulse voltage from the writing electrodes is impressed on the ferroelectric body layer to polarize the ferroelectric body layer into either a positive or negative state,
the polarization being stored in the ferroelectric body layer in a non-volatile way,
pulse voltage from the reading electrodes being impressed on the piezoelectric body layer,
wherein stress generated by an inverse piezoelectric effect due to this voltage impression is exerted on the ferroelectric body layer, and the polarity of remnant polarization of the ferroelectric body layer is read out.

III. Detailed description of the invention

[Field of industrial application]

The present invention relates to a memory device using a ferroelectric body in a recording medium and its recording/reproducing method.

[Prior Art]

A memory device in which a ferroelectric body having hysteresis characterics is used as a storage medium, wherein memory cells arranged with electrodes on the vertical side of this ferroelectric body are arrayed into a two-dimensional shape, the memory cells being matrix wired to make them recordable and reproducible in an XY address mode has been known before.

A memory cell circuit based on a conventional example is illustrated in Fig. 13.

A memory circuit 1 is provided with a ferroelectric condenser 2 and an access transistor 3. The ferroelectric condenser 2 can be set up to hold a polarized state of datum "1" as shown by the downward arrow, which indicates a negative polarized state. The condenser 2 can be further set up to hold the state of the datum "0" indicated by an upward arrow. The access transistor 3 is a MOS enhancement mode device connecting a drain terminal to the terminal of the ferroelectric body condenser 2. The second terminal of the condenser 2 is connected to a drive wire 4. The gate terminal of the access transistor 3 is connected to a word wire 5 that receives a selection signal so as to select the memory circuit 1 (sic). The source terminal of the access transistor 3 transmits the data state to the ferroelectric body condenser 2 and is connected to a bit wire 6 receiving the data state from the condenser 2. When a signal based on the word line 5 is in a high state, the ferroelectric body condenser 2 is serially connected between the drive wire 4 and the bit wire 6 by making the access transistor 3 to be a turn-on state. The access transistor 3 is made to be a turn-on state with the

word line 5, then the drive wire 4 is made from 0 to a positive voltage state. When the condenser 2 is pre-set before it holds a datum "1" of negative polarized state, a threshold voltage of the drive wire 4 applies an electric field before and after the condenser 2. As shown in Fig. 13(b), this shifts from the point P(1) upward and to the right to become the polarization P3 of the condenser 2 along a hysteresis curve. If the voltage of drive wire falls, the polarization returns to the point P(0) along the upper curve.

The state "1" is read out by detecting it with a sense amplifier, but it becomes a destructive read-out because the state changes from point P(1) to point P(0) after reading. Namely, the hysteresis curve become round by reading and rewriting, generating a hysteresis loss equivalent to an area enclosed by the hysteresis curve and connected with increased power consumption. Moreover, the second time polarization is switched by the first time read-out and rewriting, and it is also undesirable from the standpoint of fatigue.

A memory device in which a ferroelectirc body is used as memory medium and an ultrasonic wave is used to read information stored in the ferroelectirc body non-destructively has been described, e.g., in Japanese Laid-Open Patent Application 49-79738, and its construction is shown in Fig. 14 (a) —(c). Fig. 14(a) is a top view, Fig. 14(b) is a sectional view, and Fig. 14(c) is a bottom view.

In the memory device, writing electrodes 12 are formed into a matrix on the top surface of a ferro-electric body layer 11 and rows of excitation electrodes 13 are formed to enclose each row of the writing electrodes 12. Moreover, discharge lines composed of two parallel electrodes 14, 15 are formed at the under surface of the ferroelectric body layer 11 in a direction perpendicular to the excitation electrodes 13 and in positions opposite to the writing electrodes 12, with shielding electrodes 16 connected to each other at the edge of components between the discharge lines. Then, memory cells of a piezoelectric transducer are formed from the excitation electrodes 13, the shielding electrodes 16 being arranged opposite thereto and the ferroelectric bodies positioned among these electrodes. A piezoelectric transducer with the electrodes 14, 15 as output terminals is formed from the writing electrodes 12 adjacent to the memory cells, the electrodes 14, 15 being

arranged opposite thereto and ferroelectric bodies being positioned among these electrodes.

In this memory device, the memory cells and the piezoelectric transducer for reading are formed in the same plane, and stress propagated in the direction of a plane is given to the adjacent memory cells by the piezoelectric transducer, and a charge is generated in response to stored information of the memory cells to change the output voltage, the change being detected on the output side of the piezoelectric transducer.

[Problems overcome by the invention]

However, aforesaid memory device shown in Fig. 13 totally inverts the remnant polarization, and inevitably becomes a destructive reading.

In a memory device shown in Fig. 14, the memory cells and the reading part were formed in the same plane, with a limit on the integration of multiple memory cells, and a large area was necessary for a large capacity. Moreover, an ultrasonic wave is propagated to the direction of the plane. Therefore the memory cells and the reading part had to be provided for each layer, even if multiple ferroelectric body layers are laminated to create a large capacity, which was troublesome in integration.

The present invention was made in view of the above circumstances and is aimed at providing a memory device and recording/reproducing method capable of reading information stored in memory cells non-destructively, simplifying circuit construction and creating a large capacity of memory by making it to be three-dimensional.

[Problem resolution means]

To solve the above problem, the present invention adopts construction having a piezoelectric body layer exhibiting piezoelectric characteristics, a ferroelectric body layer laminated on one side of the piezoelectric body layer and laminated so as to transmit the stress generated by an inverse piezoelectric effect of the piezoelectric body layer, writing electrodes that are opposite arranged by interposing the ferroelectric body layer and generating an electric field for polarizing the ferroelectric body layer into a polarized state corresponding to information to be stored, reading electrodes that are opposingly arranged by interposing the piezoelectric body layer and generating an electric field of a magnitude which generates stress to the extent that it does not destroy the polarized state of the ferroelectric body layer, and an insulator for insulating the piezoelectric body layer and the ferroelectric body layer.

As a recording/reproducing method of the memory device thus constructed, a positive or negative pulse voltage from the writing electrodes is impressed on the ferroelectric body layer to polarize the ferroelectric body layer into either a positive or negative state, the remnant polarization being stored in the ferroelectric body layer, and pulse voltage from the reading electrodes is impressed on the piezoelectric body layer, with stress generated by the inverse piezoelectric effect due to the voltage impression being exerted on the ferroelectric body layer, and the polarity of the remnant polarization of the ferroelectric body layer is read out.

[Operation]

According to the memory device based on the present invention, if a voltage for reading is impressed on the piezoelectric body layer, stress generated thereby is given to the ferroelectric body layer, and the polarity of remnant polarization of the ferroelectric body layer is read out as stored information. Accordingly, non-destructive reading becomes possible. From the fact that the piezo-electric body layer and the ferroelectric body layer are laminated, the area of the plane is reduced, the area of plane

to the total number of memory cells is further reduced and a large capacity is facilitated by increasing the number of laminations.

[Embodiments]

Embodiments of the memory device relating to the present invention are illustrated below.

Fig. 1 is a diagram showing a schematic component structure of Embodiment 1. This memory device is arranged with stripe-shaped electrodes **21**, **22** perpendicular to each other between both sides of a piezoelectric body film **20** having piezoelectric characteristics on both sides. A ferroelectric film **23** is opposingly arranged on one side of the piezoelectric body film **20** via an insulator film **24**. Stripe-shaped electrodes **25**, **26** are arranged on both sides perpendicular to each other between both sides of the ferroelectric film **23**. The stripe-shaped electrodes **21** and the stripe-shaped electrodes **25** are arranged in parallel to each other, and the stripe-shaped electrodes **22** and electrodes **26** are also arranged parallel to each other. Moreover, the stripe-shaped electrodes **21**, **22**, **25**, **26** are so arranged that intersections where the stripe-shaped electrode **21** formed on one side and the stripe-shaped electrode **22** formed on the other side of the piezoelectric body film **20** and intersections where the electrodes **25**, **26** on the side of ferroelectric film **23** correspond 1 to 1. Piezoelectric cells are formed in a portion where the electrodes **21** and **22** of the sides of piezoelectric body film **20** intersect, and memory cells are formed in a portion where the electrodes **25** and **26** of the sides of ferroelectric body film **23** intersect. Such a laminate is formed on a silicon substrate via an insulting film **27**. A peripheral circuit **29** composed of a decoder, etc. is prepared in a monolith on the substrate **28**.

Fig. 2 is a sectional view of components shown by pulling out a pair of piezoelectric cells and memory cells. A layer **30** formed at the under surface of the silicon substrate is a sound wave absorbing layer, non-illustrated in Fig. 1.

Specific constructions of the peripheral circuit **29** are shown in Fig. 3 – Fig. 5.

The memory cells arrayed into a matrix are wired as shown in Fig. 3. This circuit is constructed so that a closed circuit is formed from a selected memory cell C_L and its peripheral memory cells C_x, C_y, C_{xy}, an impressed-voltage E_a is impressed between the selected memory cells C_L and C_y, voltage given by dividing the voltage E_a into 2/3 is impressed with a voltage-dividing resistance r1 between the C_y and C_{xy}, and voltage given by dividing the voltage E_a into 1/3 is further impressed with voltage-dividing resistances r1 and r2 between the C_x and C_{xy}. Accordingly, a predetermined voltage E_a is impressed to the selected memory cell C_L, and a voltage of 1/3 E_a is impressed on the peripheral memory cells, becoming an impressed state as shown in Fig. 6, thereby preventing crosstalk to the peripheral memory cells.

As shown in Fig. 4, the stripe-shaped electrodes 21, 22 formed on both sides of piezoelectric body film 20 are connected to a piezoelectric address decoder 41, and the stripe-shaped electrodes 25, 26 formed on the both sides of ferroelectric body film 23 are connected to a ferroelectric body address decoder 42. A reading voltage impression circuit 43 is connected to the piezoelectric body address decoder 41, and a writing voltage impression circuit 44 is connected to the ferroelectric body address decoder 42. Voltage generated in the memory cells constructing the ferroelectric body matrix is detected by a detection circuit 45, the detection signal being sent to a host computer 46. A command signal is given from the host computer 46 to the piezoelectric body address decoder 41 and the ferroelectric body address decoder 42.

Fig. 5 is an example in which the circuit shown in Fig. 3 and the circuit shown in Fig. 4 are combined to construct a driver circuit of the memory cells and piezoelectric cells. Moreover, specific operations for selecting and driving cells are described in detail in Japanese Patent Application S63-32163, and therefore are omitted here.

When a memory device thus constructed is manufactured, the peripheral circuit shown in Fig. 5 beginning with the decoder is formed into a monolith on a silicon substrate 28 coated with a sound wave absorbing layer 30 at the back. An insulting film 27 is further formed on the substrate 28. The

lower electrodes 26 of Pt, Au, etc. are formed into a stripe shape on the insulting film 27, one end of which is connected to the peripheral circuit. The ferroelectric body film 23 of PZT (plumbic silicotitanate), PT (plumbic titanate), etc. is imparted to the lower electrodes 26 by the sol-gel process, spin coating or sputtering process. Subsequently, a perovskite crystal film free of pyroclore phase (ferroelectric body film 23) is formed by heat treatment, and the stripe-shaped upper electrodes 25 made of either Pt or Au, etc. are imparted onto the film. Next, the PZT is formed with Ta_2O_5, Si_3N_4 or $BaTiO_3$ as the insulator film 24. Moreover, the stripe-shaped lower electrodes 22 made of either Pt or Au, etc. are imparted onto this insulator film 24, and the piezoelectric body film 20 made of PZT, PT, etc. is further formed by the same technique, thereby forming the stripe-shaped upper electrodes 21. Furthermore, a silicone resin evenly dispersed with tungsten fine particles is coated so as to cover the upside of piezoelectric body film 20, the back of ferroelectric body film 23 and the edge of piezoelectric body film 20 and ferroelectric body film 23.

The memory circuit 1 shown in Fig. 1 is obtained by the above process.

An explanation is provided here of the relationship between the memory cells using a ferroelectric and the stress given to these memory cells (ultrasonic wave in the case of this embodiment).

PZT ceramic comprising a typical ferroelectric body is polarized by impressing an electric field of over coercive electric field E_c, and the polarized state is maintained even after stopping the impression of voltage. The magnitude of the piezoelectricity held by the ferroelectric body relates to the magnitude of the remnant polarization P_r. If the operating voltage and input energy given to the ferroelectric body are reduced, the polarized state of the remnant polarization P_r is not destroyed.

A 0.2 mm-thick PZT ceramic formed with electrodes on both sides is considered as one example. If a polarization voltage of about 800 V is applied to accomplish polarization, and then an alternate-current voltage is impressed, voltage in the direction of depolarization is also impressed because the voltage is alternating-current voltage, but actually it is not depolarized, although the polarization voltage is dependent on the material PZT. Therefore, if the cells are driven by a voltage lower than

the polarization voltage, the polarized state is not inverted or destroyed.

The case of impressing a voltage was illustrated, and a case of applying a stress is similarly considered. Namely, a remnant polarization P_r is generated by impressing a voltage higher than the voltage V_c in the hysteresis characteristic shown in Fig. 11 on a ferroelectric body (having piezoelectricity) shown in Fig. 10. If a stress T is applied to the ferroelectric body thus polarized and the thickness changes by Δt, a voltage V_{out} generated by it is obtained by the following equation:

$$V_{out} = d_{33} \cong T / \varepsilon \qquad (1)$$

Although the instantaneous remnant polarization P_r applied with a stress somewhat changes, if the stress T is removed, it returns to the original state P_r again. At this time, the following relationship exits among the polarity of applied stress ($T > 0$, $T < 0$), the polarity of polarization P_r and the polarity of generated voltage V_{out}.

Polarization	Stress	Generated Voltage
$P_r > 0$	Pressure	$V_{out} < 0$
	Tensile force	$V_{out} > 0$
$P_r > 0$	Pressure	$V_{out} < 0$
	Tensile force	$V_{out} > 0$

If the generated voltage in applying the same stress is found from this relationship, the polarity of polarization P_r can be determined. Actually, when alternative stress, e.g., an acoustic vibration or a voltage acoustic vibration is impressed, the polarity of polarization P_r is determined by whether the phase of generated alternating-current voltage conforms with the phase of ultrasonic vibration or becomes an inverse phase.

The appearance of stress, generated voltage and polarization polarity are shown in Fig. 12(a) – (c). When a ferroelectric body is a positive remnant polarization P_r, the generated voltage in applying the stress has a positive polarity. When a ferroelectric body has a negative remnant polarization P_r,

the generated voltage is negative polarity. The ferroelectric body memory shown in Fig. 12 is one layer, but this is the same in the case of two or more layers. Only one cell is modally written, but the same effect is obtained in a high-density memory which is made into a two-dimensional matrix. At this time, however, it is desirable to use a ferroelectric material with a small Pois-son's ratio, e. g., it is desirable to use $PbTiO_3$ to suppress crosstalk.

In such an embodiment, when data are written into predetermined memory cells, a write command from the host computer 46 is sent with an address and the written memory cells are selected by the ferroelectric body address decoder 42. Write voltage E_a is impressed from the write voltage impression circuit 44 onto the memory cells selected by the ferroelectric body address decoder 42. At this time, only a charge of 1/3 E_a is impressed on the peripheral memory cells by the circuit shown in Fig. 3. As a result, information is written into the selected memory cells without destroying the memory status of the peripheral memory cells.

Next, when the data are read from the predetermined memory cells, a read command from the host computer 46 is sent with an address to the piezoelectric address decoder 41, and voltage is impressed from the reading voltage impression circuit 43 to the piezoelectric cells in the address. An ultrasonic wave is propagated from the piezoelectric cells to the selected memory cells with this impression of voltage. A change of voltage generated in the selected memory cells according to this stress wave is detected by the detection circuit 45, this detection signal is sent to the host computer 46 and accordingly the data are read off.

By such an embodiment, the information of memory cells can be read out non-destructively because the piezoelectric body film 20 is laminated onto the ferroelectric body film 23, ultrasonic wave (stress) is given to each memory cell of the ferroelectric body film 23, and voltage differences caused by differences in information accumulated in each memory cell can be detected. Moreover, the destruction of the memory status of peripheral memory cells by crosstalk can be surely prevented because the impression of writing voltage onto each memory cell is carried out by the circuit shown in Fig. 3.

Moreover, the memory cells can be prepared into a high density and a large capacity can be created as compared with a memory device in which the memory part and the reading part, as shown in Fig. 14, are formed in the same plane because the piezoelectric body film 20 is laminated onto the ferroelectric body film 23 in this embodiment.

Embodiment 2 of the present invention is described next..

Fig. 7 is a diagram showing a schematic component structure of a memory device of Embodiment 2. Moreover, it is shown by attaching the same symbols to parts having the same functions as in Embodiment 1. This memory device adopts such a construction that the insulator film 24 shown in Fig. 1 is removed, and the lower electrodes 22 of piezoelectric body film 20 and the upper electrodes 25 of ferroelectric body film 23 are common intermediate electrodes 31.

When this memory device is manufactured, a peripheral circuit like Fig. 5 is formed into a monolith on a silicon substrate 28. Then, stripe-shaped electrodes 26 made of Pt, Au, etc. are formed by means of a sputtering process via an insulting layer 27 of SiO_2, etc. formed on the silicon substrate 28. Then, PZT or PT, etc. are formed as the ferroelectric body film 23 by the sol-gel process or sputtering process, etc. preferable use being made of PT having a small Poisson's ratio. The ferroelectric body film 23 is so formed is annealed at nearly 600°C in an oxygen atmosphere to become a perov-skite single-phase crystal and then stripe-shaped common intermediate electrodes 31 become perpendicular to the lower electrodes 26. The common intermediate electrodes 31 and electrodes 26 are connected to a ferroelectric body address decoder. PZT, PT, etc. are formed on these common inter-mediate electrodes 31 as the piezoelectric body film 20 by means of the sol-gel, sputtering process, etc. PZT with a high piezoelectricity is preferably used. For combinations of ferroelectric body film material and piezoelectric body film material here, the former is preferably of a high coercive electric field type such as PT, etc. and the latter is preferably of a low coercive electric field type such as PZT, etc.

Next, the stripe-shaped electrodes 21 are imparted to the piezoelectric body film 20 by the same method. The stripe-shaped electrodes 21 are connected to a piezoelectric body address decoder for excitation of piezoelectric cells, comprising the piezoelectric body address decoder, ferroelectric body address decoder and the first – third address decoder, the first address decoder is connected to the lower electrodes 26, the second address decoder is connected to the common intermediate electrode 31, and the third address decoder is connected to the upper electrodes 21.

The memory device shown in Fig. 7 is manufactured as above.

Fig. 8 is a component sectional view shown by pulling out a pair of piezoelectric cells and memory cells of the memory device relating to the embodiment.

The operation of this embodiment are described next. First, all of the memory cells and all of the piezo-electric cells are initialized into a state of "1". Moreover, if all of the piezoelectric cells are in the same polarized state, they may not necessarily be in a state of "1", i.e., a state of Pr. Initialization can make the upper electrodes of ferroelectric body film 23 and the lower electrodes of piezoelectric body film 20 into the state of "1" through the second address decoder at a stroke because the electrodes are in common (common intermediate electrode 31).

Next, writing is carried out as described below. A predetermined memory cell is selected through the first and second address decoder (ferroelectric body address decoders). When writing "1" → "0" is carried out, a voltage $+V_{\pi}$ (unclear letter, translator) of polarity reverse to a voltage $-V_{\pi}$ needed for initialization is impressed. At this time, a voltage of same potential as the common intermediate electrode 31 is impressed on the corresponding piezoelectric cell through the third address decoder so that a voltage of polarity reverse to the voltage V_{π} is not applied to the piezoelectric body cell. The third address decoder always selects an electrode line of same address as the address selected by the first address decoder.

In the manner described above, the writing into a specific memory cell can be made without changing the polarized state of piezoelectric cell.

The read operation is described next.

An impressed voltage which does not destroy the polarized state of piezoelectric cells is impressed onto the piezoelectric cells. For example, if the impressed voltage is V, the piezoelectric constant d_{33}, the Young's modulus Y, the surface area of piezoelectric cell S and the thickness d, the stress F is expressed by:

$$F = (S/d)\, d_{33} Y \equiv V$$

If the voltage is pulse, it is transmitted to a corresponding memory cell in the form of vibration. The memory cell receives this vibration and distorts it, and generates a charge at the electrode surface due to the piezoelectric effect. When the dielectric constant of ferroelectric body is ε, the generation of the charge is expressed by $V = d/\varepsilon F$; when this charge is detected by its polarity or by a circuit of low impedance, the read-out of memory state can be established by the polarity of current.

Such an Embodiment 1 enables a non-destructive reading similarly as the above Embodiment 1.

Subsequently, Embodiment 3 of the present invention is illustrated.

Fig. 9 is a diagram showing Embodiment 3. In this embodiment, only one layer of a piezoelectric body film 51 is formed on a substrate 50, on which multiple layers of insulating film 52 and ferroelectric body film 53 are laminated. Electrodes are formed on both sides of the piezoelectric body film 51 and ferroelectric body film 53, respectively. This embodiment becomes such a construction that multiple memory cells composed of a ferroelectric body and electrodes interposed by this ferroelectric body are formed in the direction of lamination, forming one piezoelectric cell

giving a stress to these multiple memory cells. Such laminated multiple memory cells and one piezoelectric cell are arrayed two-dimensionally, and addresses are similarly selected by stripe electrodes as the embodiments.

According to Embodiment 3, a stress wave (ultrasonic-wave) caused by the piezo-electric body film **51** propagates in the direction of lamination of ferroelectric body film **53** (sic) and acts on memory cells of same address of each layer. These memory cells of same address are selected by an address decoder connected to each layer, an output from these cells is input into a sense amplifier, and its output polarity is detected by a detection circuit, the detected polarity corresponding to information stored in each layer, therefore memory information of each layer is read out.

Although the voltage impressed on the piezoelectric body film **20** is taken as a reference in Embodiment **2**, if the voltage impressed on the piezoelectric body film **51** is taken as reference as it is in this embodiment, a layer apart from the piezoelectric body film **51** causes a difference until the stress wave is reached, and time sometimes cannot be added.

Accordingly, the embodiment is so constructed that non-polarization inverted dummy cells are arranged in each layer formed with the memory cells, and output from the dummy cells of each ferroelectric body film **53** generated by the stress wave due to dummy cells of the piezoelectric body film **51** is used as a reference.

This example is described in detail according to Fig. 9 below. Dummy cells **531, 532, 533** are arrayed immediately above the cells **51** for excitation of dummy cells generating the stress wave, and all of memory cells **611, 612, 613** use the same ferroelectric body thin film. Namely, all the dummy cells **531, 532, 533** are made into a polarized state of same direction, and the memory cells determine the direction of polarization in accordance with the store-status. Both the cells **51** for excitation of dummy cells and the cells **60** for non-destructive reading of the memory cells **611, 612, 613** are in the same piezoelectric thin film, and voltage of same phase and same amplitude is impressed by the same timing during the excitation. If so, for example, if the polarized state of the

memory cell 611 is a polarized state of the same direction as the direction of polarization of the dummy cell 531, the read-out waveform of the memory cell 611 is nearly the same as the read-out waveform of the dummy cell 531. Therefore, the direction of polarization of memory cell judged by the direction of polarization of a dummy cell, i.e., the stored-status is known by taking a working output of both outputs. Moreover, this is the same in relation to the memory cell 612 and the dummy cell 532 on a single layer. An insulating thin film 52 is formed to prevent a short between the striped electrodes and the layers, and this condition is also the same in the dummy cell. Thereby, the higher the layer, the more disordered waveform the stress wave reading is, accordingly there appears to be a meaning for detecting a difference between the dummy cells and the memory cells in each layer. Furthermore, the piezoelectric stress wave excited from reading piezoelectric cells 60 is somewhat deformed by propagating through the memory cell layers, but the polarity does not change. Therefore, the memory state of each layer is read out accurately and non-destructively.

[Efficacy of the invention]

As described in detail above, the present invention enables providing a memory device and its recording/reproducing method which can read out information stored in memory cells non-destructively, simplify the circuit construction and contrive a large capacity by forming three dimensions.

IV. Brief description of the drawings

Fig. 1 is a diagram showing the schematic construction of the memory device of Embodiment 1.

Fig. 2 is a component sectional view of the same embodiment, Fig. 3 and Fig. 5 are peripheral circuit diagrams of the same embodiment.

Fig. 6 is a diagram showing a voltage impressed state of selected memory cell and their peripheral cell.

Fig. 7 is a diagram showing the schematic construction of the memory device of Embodiment 2.

Fig. 2 is a component sectional view of the same embodiment.

Fig. 9 is the component sectional view of Embodiment 3.

Fig. 10 is a diagram for illustrating a relationship between the stress given to a ferroelectric body and the generated voltage.

Fig. 11 is a diagram showing the hysteresis characteristic of the ferroelectric body.

Fig. 12 is a diagram showing a relationship between the remnant polarization and the generated voltage of the ferroelectric body.

Fig. 13(a) is the circuit board of a memory cell.

Fig. 13(b) is an operating illustrative diagram of the same circuit diagram, and Fig. 14 is a diagram showing the memory device using piezoelectric components.

20	piezoelectric body film
21, 22, 25, 26	striped-shaped electrodes
23	ferroelectric body film
24, 27	insulting films
28	silicon substrate
29	peripheral circuit
30	sound wave absorbing layer

Fig. 1

Fig. 2

Fig. 3

20, 21, 22	piezoelectric body matrix
23, 25, 26	ferroelectric body matrix
41	piezoelectric address decoder
42	ferroelectric address decoder
43	reading voltage impressing circuit
44	writing voltage impressing circuit
45	detecting circuit
46	host computer

Fig. 4

Fig. 7

Fig. 8

(right, from top)

electrode electrode ferroelectric body film substrate

Fig. 9

ferroelectric body

Fig. 10

(horizontal) Polarization value Impressed voltage

Fig. 11

Fig. 12

Fig. 13

Fig. 14